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WHAT IS CLAIMED IS:

A circuit for glitch-free changing of clock having different phases, wherein the circuit receives M clocks labeled by $1\sim M$ and at least one data stream, in which the M clocks have the same frequency and are different in phase sequentially, and one of the M clocks (labeled by N, $1 \leq N \leq M$) is selected to be a system clock, the circuit comprising:

- a phase detector for receiving the data stream and the system clock, and generating a phase-up signal and a phase-down signal;
- a flag signal generator coupled to the phase detector for receiving the phase-up signal and the phase-down signal, and then generating M flag signals, wherein only one of the M flag signal is substantially enabled at the same time;
- a select signal generator coupled to the flag signal generator, for receiving the M flag signals and the M clocks to correspondingly generate M select signals; and

an output stage coupled to the select signal generator, for receiving the M select signals and the M clocks, and then outputting the system clock, wherein the outputted system clock corresponds to one of the M clocks selected by the enabled select signal.

- 2. The circuit of claim 1, wherein when the phase of the data stream lags behind the phase of the system clock, the phase-up signal is enabled, and when the phase of the data stream leads the phase of the system clock, the phase-down signal is enabled.
- 3. The circuit of claim 1, wherein under the condition of clock N being at a first level, when the phase-up signal is enabled, the flag signal N+1 is enabled; and when the phase-down signal is enabled, the flag signal N-1 is enabled.
 - 4. The circuit of claim 3, wherein the first level is a low level.
 - 5. The circuit of claim 1, wherein a high level is defined as being enabled.

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- 6. The circuit of claim 1, wherein the flag signal generator is a ring counter.
- 7. The circuit of claim 1, wherein the select signal generator comprises M low pass latches, and each of the M low pass latches comprises a clock input, a signal input, and an output.
- 8. The circuit of claim 7, wherein, for the Nth latch, its clock input correspondingly receives the clock N, the signal input correspondingly receives the flag signal N and the output correspondingly outputs the select signal N, and when the clock N is at a first level, the select signal N substantially outputs the same level with the flag signal.
 - 9. The circuit of claim 8, wherein the first level is a low level.
- 10. The circuit of claim 1, wherein the select signal generator comprises M D-type flip-flops, and each of the D-type flip-flops comprises a clock input, a signal input, and an output.
- 11. The circuit of claim 10, wherein each of the D-type flip-flop is triggered at a rising edge.
- 12. The circuit of claim 10, wherein, for each D-type flip-flop, its clock input correspondingly receives the clock N, the signal input correspondingly receives the flag signal N and the output correspondingly outputs the select signal N, and when the clock N is at a first level, the select signal N substantially outputs the same level with the flag signal.
 - 13. The circuit of claim 12, wherein the first level is a low level.
 - 14. The circuit of claim 1, wherein the output stage further comprises:
- M OR-gates, each of the OR-gate receiving each of the M select signals and each of the corresponding M clocks; and

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an AND-gate, for receiving outputs of the M OR-gates and outputting the system clock.

1 A method for changing clock having different phase without glitch, used for receiving M clock and at least one data stream and then outputting a system clock, wherein the M clocks have the same frequency but are different in phase sequentially, and one of the M clocks (labeled by clock N, $1 \le N \le M$) is currently the system clock, the method comprising the steps of:

- a. determining the phase of the data stream, and proceeding to a next step b if the phase of the data stream is changed, otherwise repeating step a;
- b. enabling a flag signal N+1 corresponding to the clock N+1 and then proceeding to a step c when the phase of the data stream lags behinds the phase of the system clock;
- c. enabling a flag signal N-1 corresponding to the clock N-1 and then proceeding to a step d when the phase of the data stream leads the phase of the system clock and the system clock is at a first level;
- d. enabling a select signal N+1 corresponding to the flag signal N+1 and then proceeding to a step f, when the clock N is at the first level;
- e. enabling a select signal N-1 in response to the flag signal N-1 and then proceeding to a step g, when the clock N is at the first level;
- f. setting the clock N+1 as the system clock and increasing N by one, and then returning to the step a; and
- g. setting the clock N-1 as the system clock and decreasing N by one, and then returning to the step a.
 - 16. The method of claim 15, wherein a high level is defined as being enabled.

17. The method of claim 15, wherein the first level is a low level.